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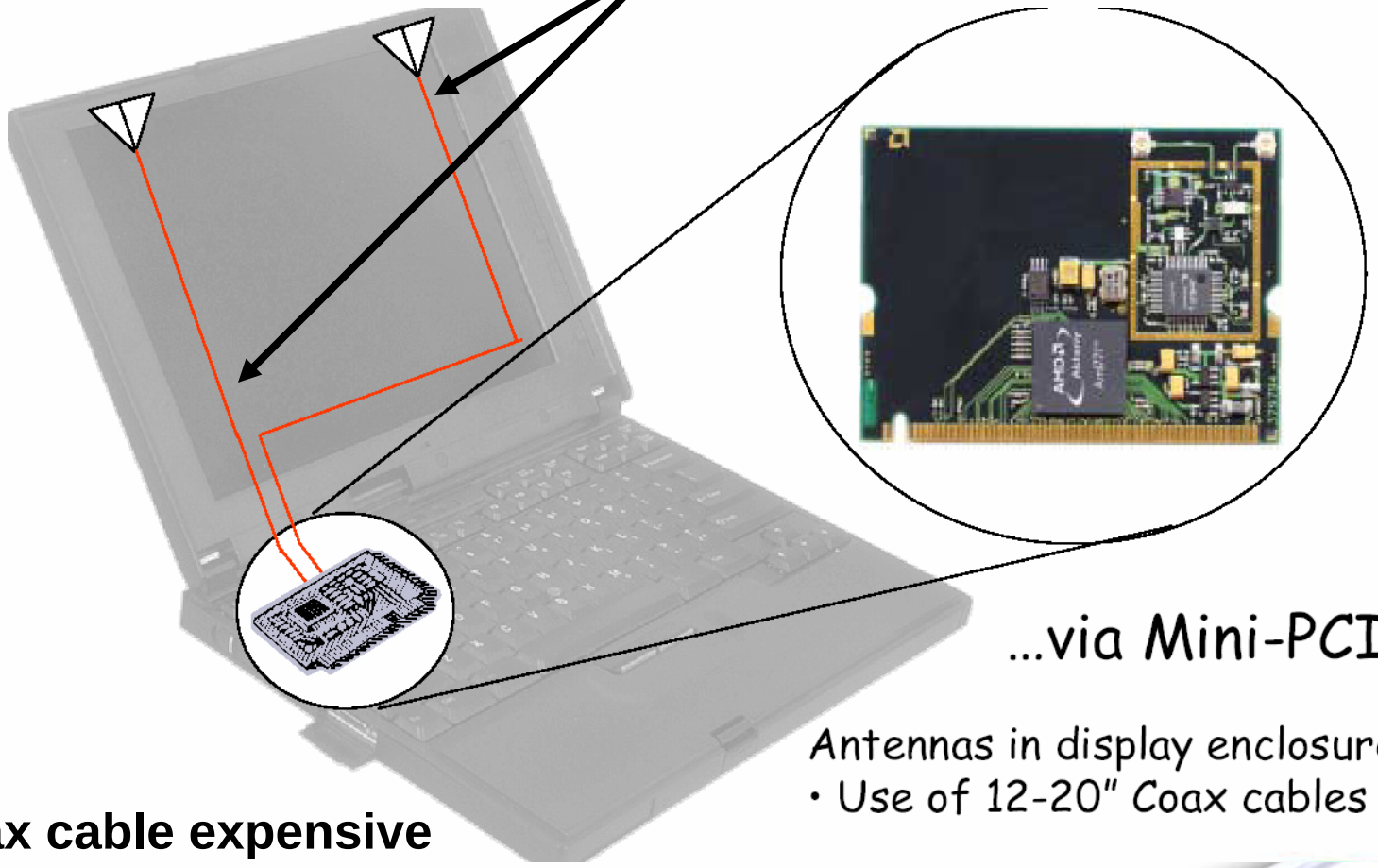
NVIDIA Wireless LAN

Introduction of Digital Radio

Ed Liu

Current WLAN Implementation
Analog Radio

50cm coax cable loss is 2dB@2.4GHz, 6dB@ 5GHz



...via Mini-PCI

Antennas in display enclosure
- Use of 12-20" Coax cables

Coax cable expensive

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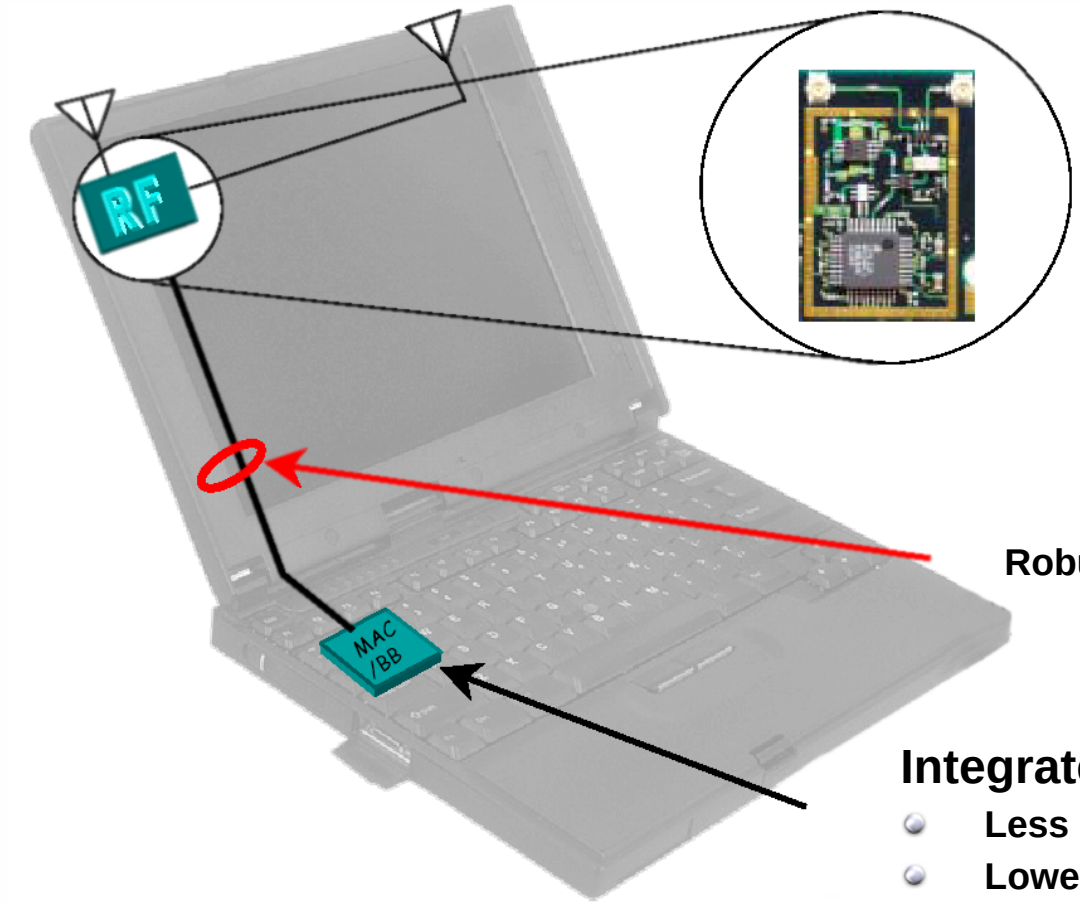
Future WLAN Implementation
Digital Radio



RF Module

- Small Size
- Minimize signal loss
- Low cost
- Possible co-location of antenna on module

Robust digital interface

Integrated MAC/BB

- Less susceptible to interference
- Lowers WLAN cost

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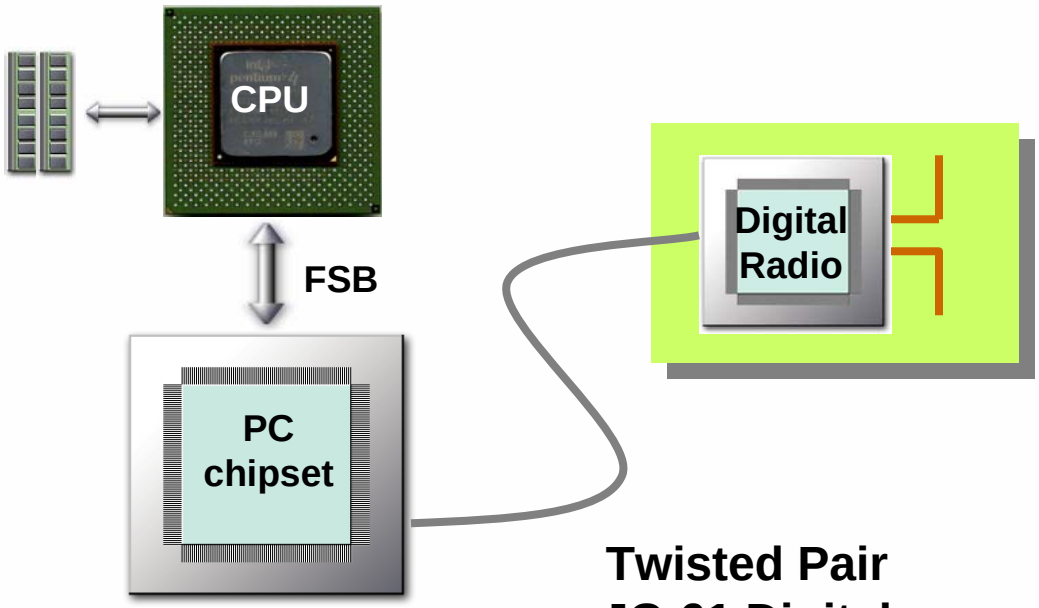
Digital Radio



- Lower Cost
- Higher Performance
- Simpler Assembly
- Printed Antenna
- Lower Power

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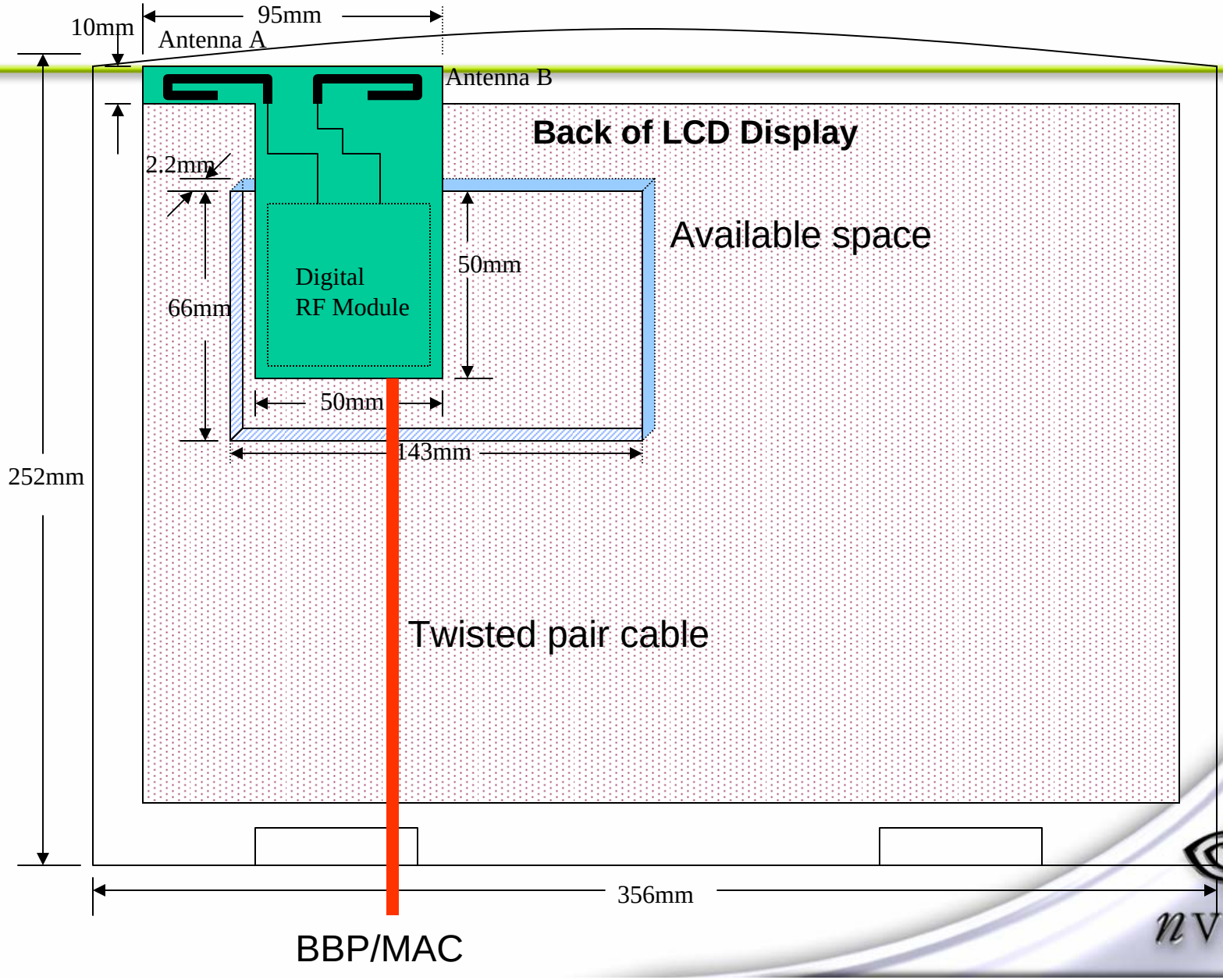
New Solution with Digital Radio



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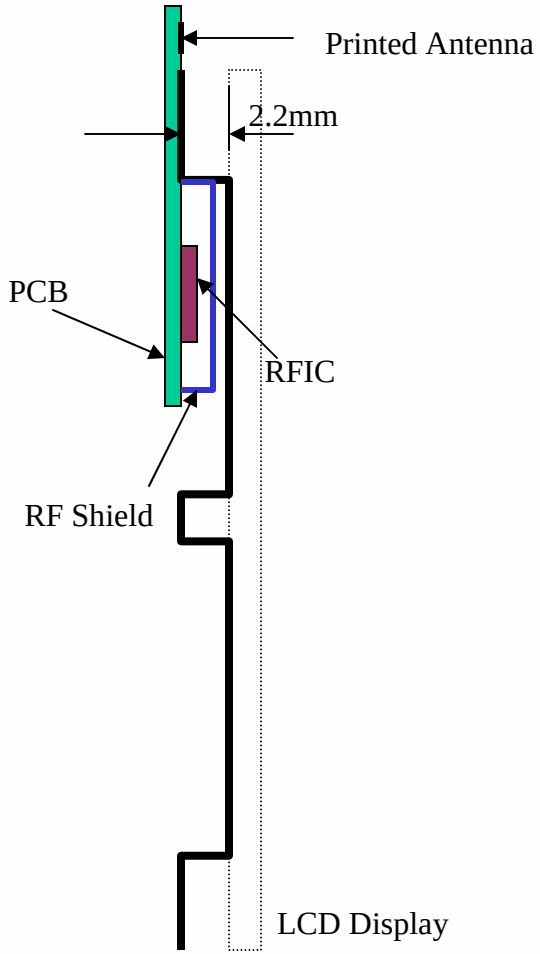
RF Module Cross-section View



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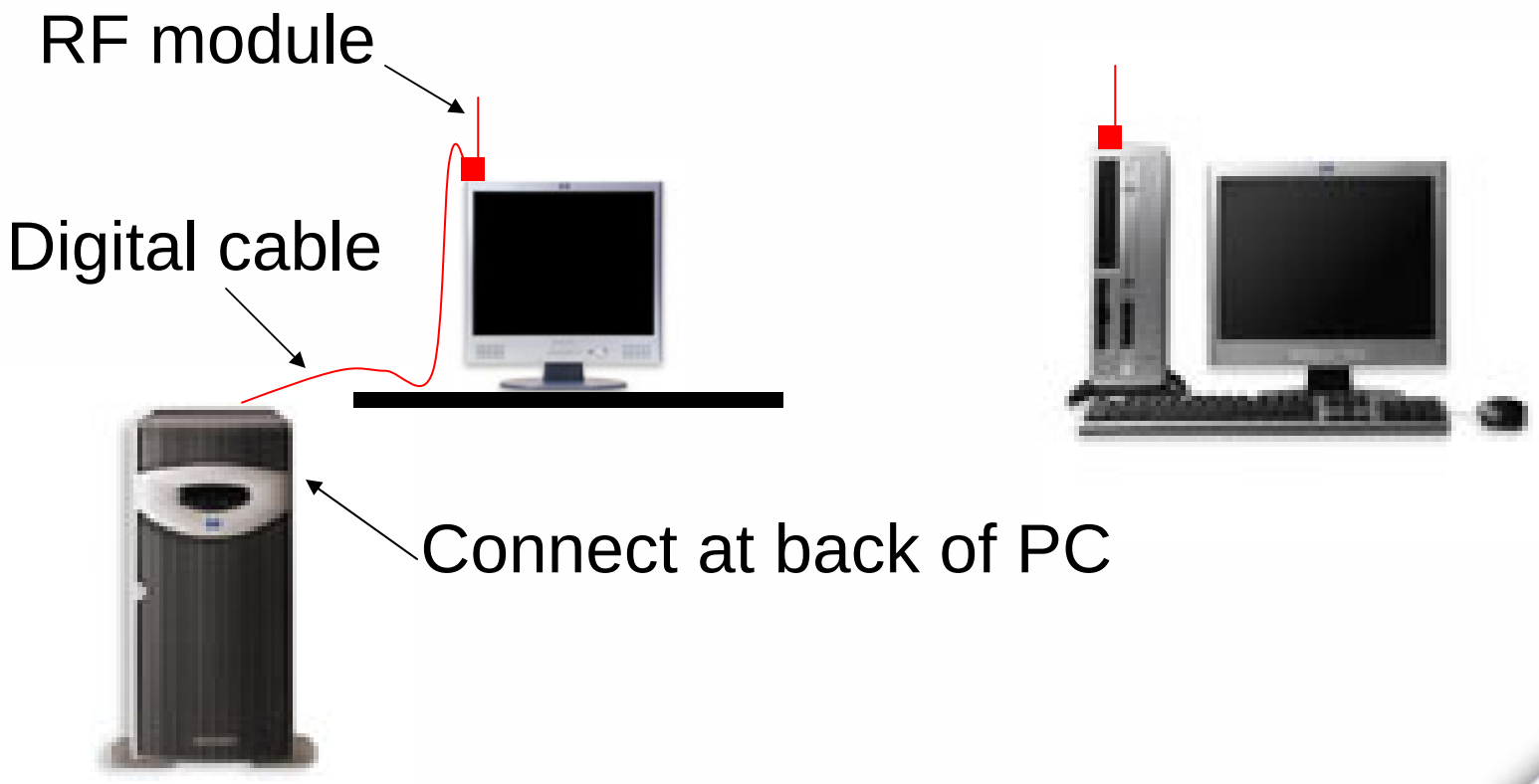
Zero-Loss Digital Cable Enables Flexible Placement



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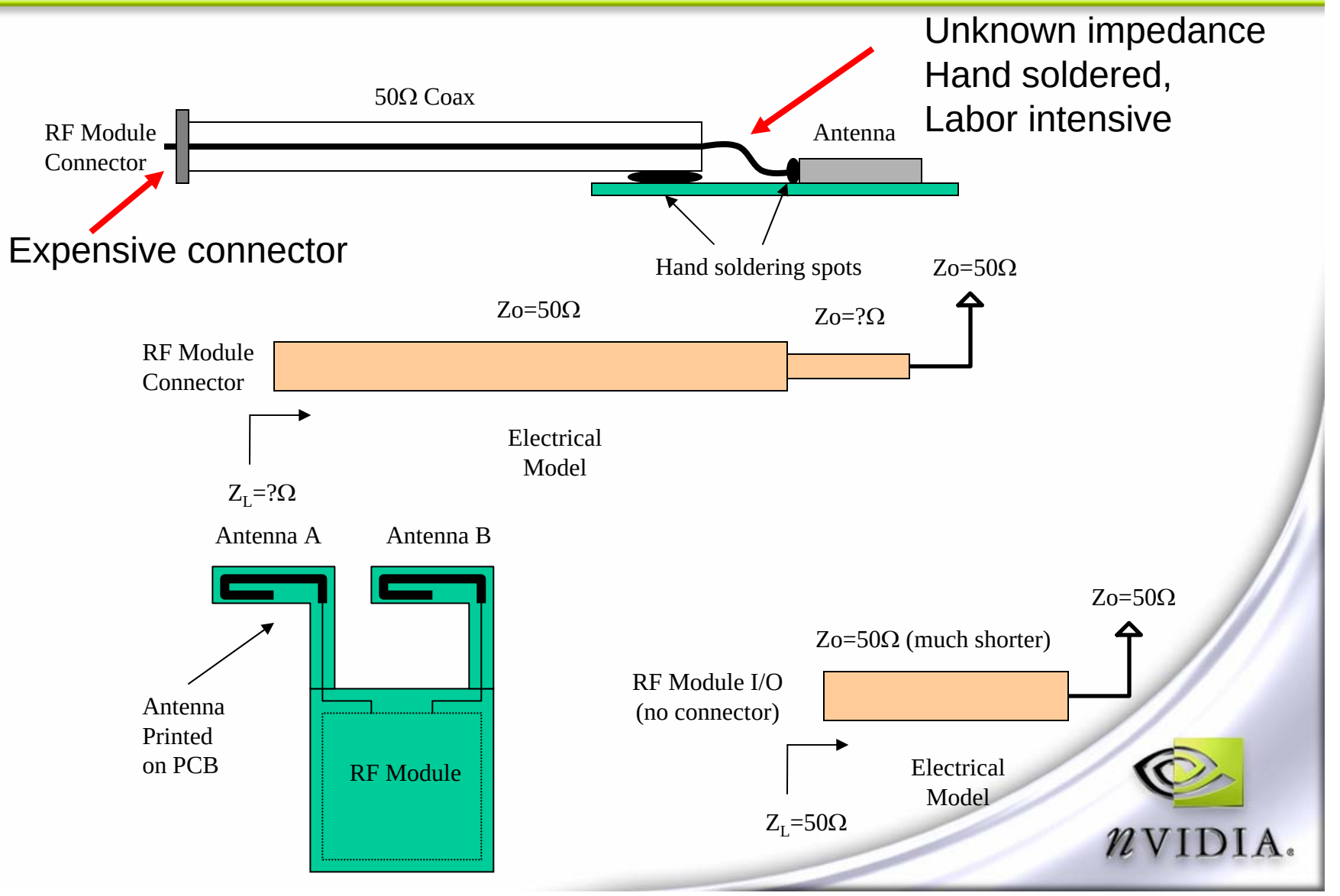
Simpler Assembly, Better Matching



Summary - Digital Radio Ideal for Laptops

- At back of LCD screen, Digital Radio has
  - Better reception
  - Less CPU heat
  - Less noise
  - Less vibration from fan
- Increase range and lower costs
  - Digital cable has no signal loss and costs less
- Printed antenna easy to manufacture
- Flexible antenna placement

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FCC Certifications
5/23/05

What Do We Plan To Certify

- We plan to certify RF module and BBP/MAC FPGA together as a “partitioned module”
- The goal is to have a single certified RF module that can work with same BBP/MAC embedded in different systems and physical implementations
  - Enables early FCC certification so that product development cycle is reduced for overall system
  - Reduces need to re-certify systems even when same BBP/MAC implemented in different chips. Many system chips have variations in portions not related to wireless

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Can We Approve RF Module as Modular Transmitter

- Currently, DA 00-1407 requires that
  - Only modulation data can be input to modular transmitter
  - Control signals cannot be input
- Traditionally, only miniPCI, Cardbus, or USB interface satisfies this requirement
- This forces BBP/MAC to reside on the RF module
- With latest digital technology, it is lower cost and power to embed BBP/MAC into another system
- Applications include laptops and cell phones

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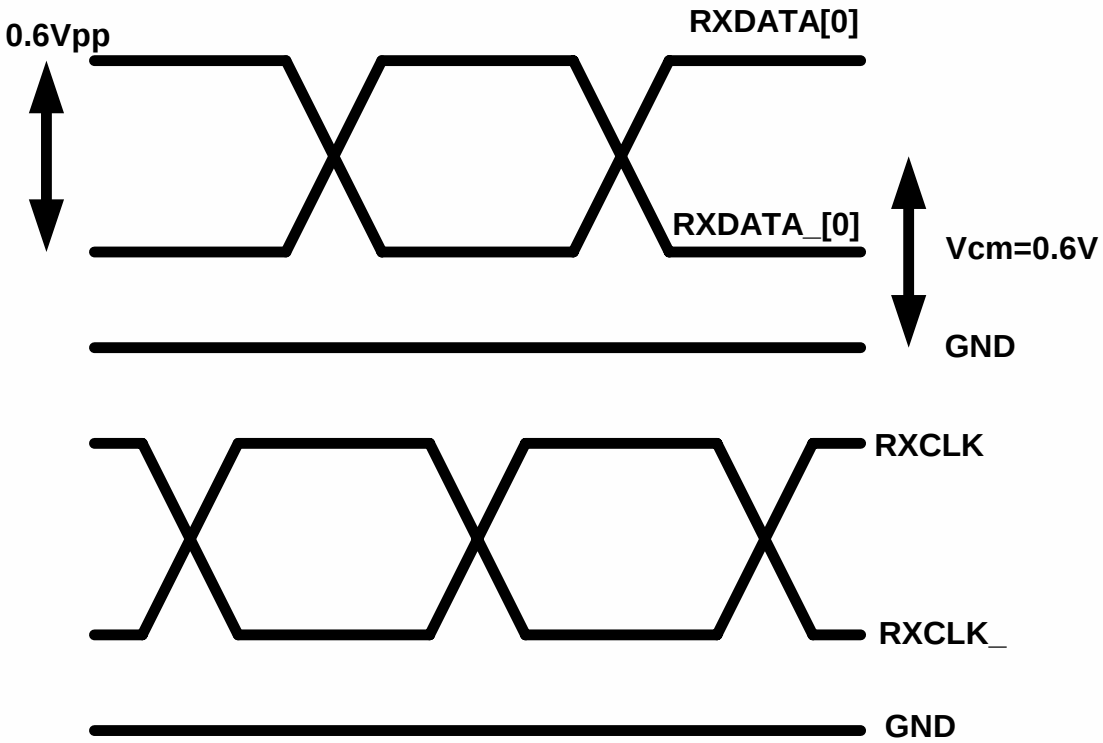
How to Ensure Noise Immunity of Data Lines between RF and FPGA

- **Robust electrical signaling**
  - **Adopted JC61 (HyperTransport) electrical signaling**
  - **HyperTransport has been used in all existing AMD processors being shipped**
- **Real-time, self-check capability for data lines to detect critical link errors**

JC61 Electrical Characteristics



- 100 ohm impedance
- Differential signaling
- 0.6V common-mode, 0.6Vpp swing

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Data Link Self-Check Capability

- Critical radio control from BBP/MAC performed via register programming command
  - Tx, Rx, Idle mode selection
  - Channel selection
  - Power level selection
  - Antenna selection
- When each command completes, the radio will echo the command back to BBP/MAC for verification
- BBP/MAC will check for the echo and make sure it matches with the original command
- If not, then BBP/MAC knows there is a link error and will power down radio and perform system reset

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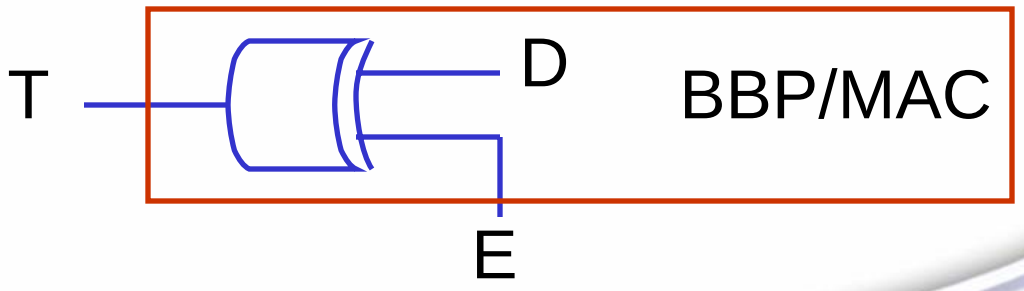
Means to Ensure Specific FPGA Implementation Matches with RF Module

- FPGA will verify device ID on RF chip at initialization
- The JC-61 committee has approved an industry wide standard for a digital interface between radio front-end and digital radio controller
- The JC-61 standard defines a 4 byte value separated into a 2 byte manufacturer's JEDEC-assigned ID code and a 2 byte device type

Means to Inject Errors into Digital Link for Robustness Test

- Robustness of digital link can be checked by injecting random bit errors
- Because BBP/MAC controls radio, link direction from BBP/MAC to radio is most important
- A random bit error can be injected using an XOR circuit on the BBP/MAC
- D is normal data from BBP/MAC to radio. If E is enabled randomly from an external source, the XOR circuit flips the polarity of the bit, D, randomly to produce corrupted output T for transmission to radio



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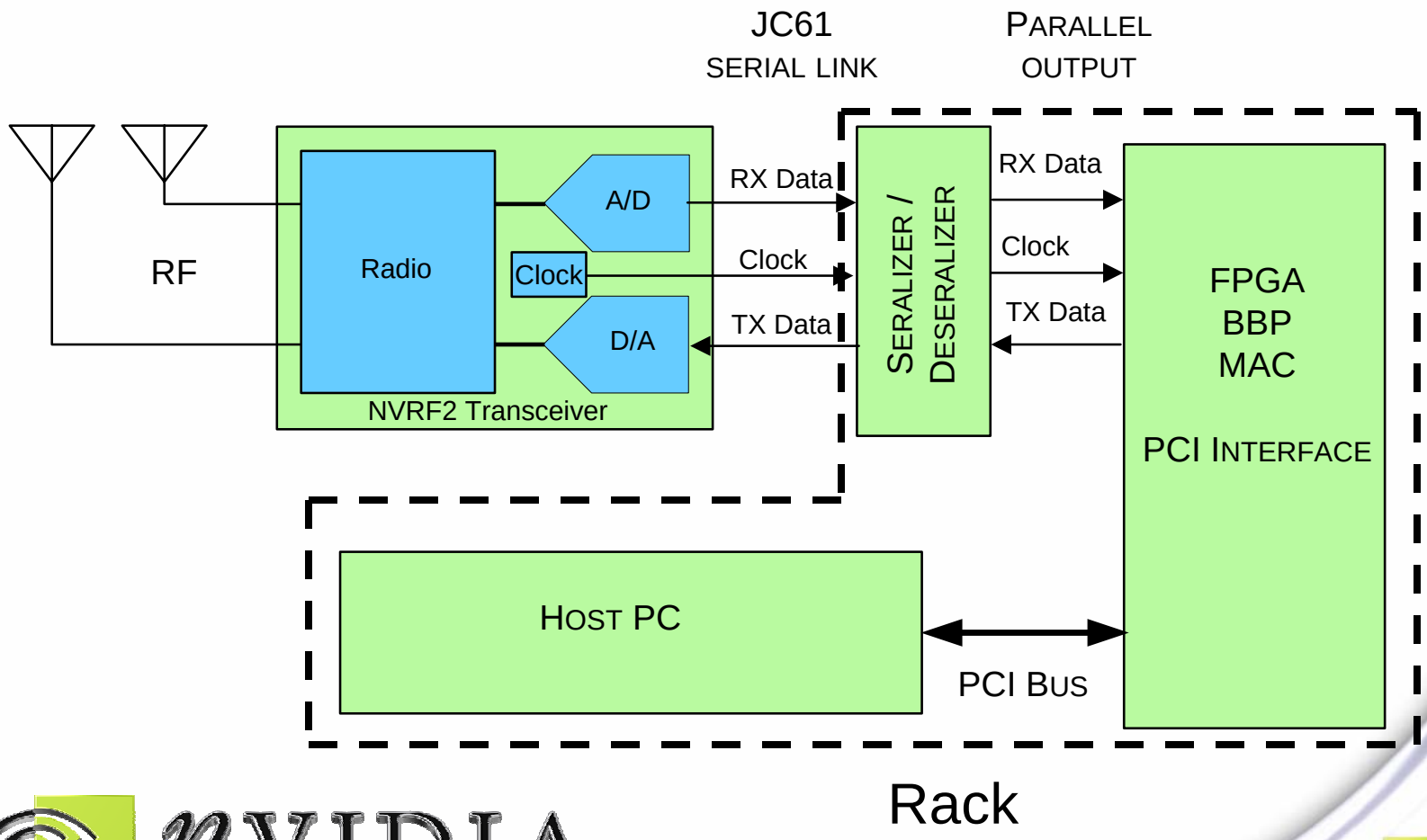
Schematic Block diagram



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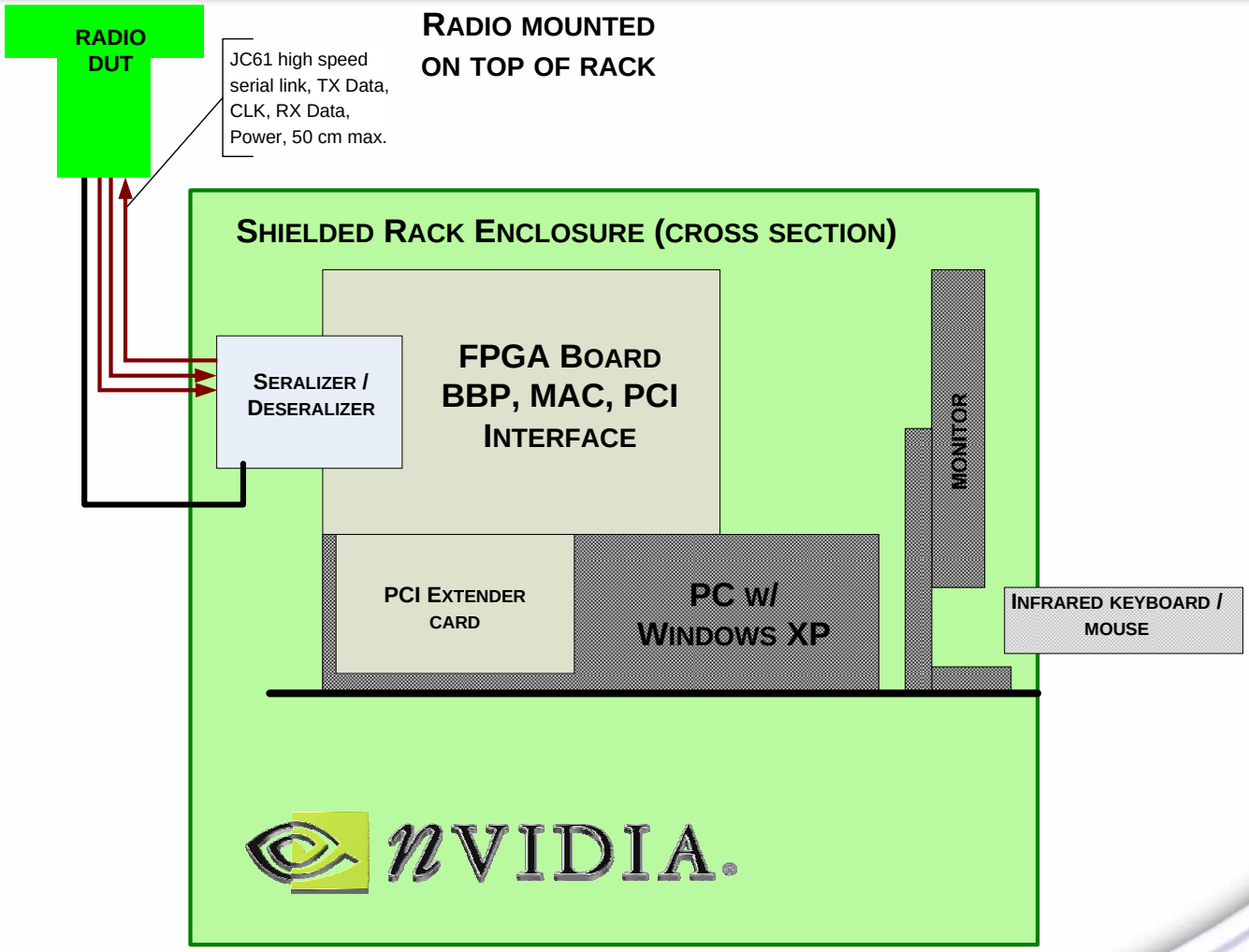
Physical Diagram of Rack



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